

## About VIT

VIT University (previously vellore engineering college) is the most prestigious private university in India under the able chairman ship of the visionary Dr G Vishwanathan. It was established with the aim of providing quality higher education on par with international standards persistently seeking and adopting innovative methods to improve the quality of higher education on a consistent basis. The campus has a cosmopolitan atmosphere with students from all corners of the globe. The global standards set at VIT in the field of teaching and research is at par with any standard Indian university.

## MEMS

Micro-Electro-Mechanical Systems (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. While the electronics are fabricated using integrated circuit (IC) process sequences (e.g., CMOS, Bipolar, or BICMOS processes), the micromechanical components are fabricated using compatible "micromachining" processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices.

Researchers in MEMS use various engineering software tools to take a design from concept to simulation, prototyping and testing. Finite element analysis is often used in MEMS design. VIT has started its MEMS design activities in 2002. Gradually, VIT has

been enhancing its research activities by setting up a MEMS design centre under the sponsorship of NPMASS.

## IntelliSuite

IntelliSense's software architecture is based upon a unique combination of the best of bottom-up process-driven design and topdown synthesis. Top-down methodology allows you to quickly explore a wide range of design options, while bottom-up design provides the accuracy to produce first-time-right silicon. IntelliSense gives you a distinctive methodology to tackle conversion of product specifications and requirements into a working product. The accurate bottom-up process-driven design and top-down schematic-driven synthesis are combined for faster designing with less process iterations

IntelliSuite allows us to design and analyze devices at different levels. Core computational engines and databases combined with synthesis, optimization, process modeling, physical and system model extraction provide a friction-free and efficient workflow.

IntelliSuite's bottom up architecture is based upon process elements — familiar process steps, such as photolithography, thin film deposition, and selective etching form the basis of understanding the final device geometries.

In addition, the analysis modules (fully integrated thermo-electromechanical analysis, high-frequency electromagnetic analysis, micro-fluidics analysis) can be

used to analyze the performance of MEMS models.

IntelliSuite features a comprehensive material and process database, allowing us to understand material properties like conductivity, film stresses and mechanical strength as a function of processing parameters. This enables us to produce more realistic models.

A new class of numerical algorithms based on Krylov/Arnoldi subspace reduction techniques has been developed to convert FEA models into arbitrary degree of freedom (NDOF) models. These algorithms are used to capture the total energy and energy dissipation in the system. Based on this, FEA/BEA models can be reduced to efficient compact system models that can be incorporated into system simulators.

Course goals

This course prepares you to:

- Develop your applications with IntelliSuite.
- Create new models and do necessary analysis.
- Creating FEM model of any arbitrary structure.
- Mimic fabrication process which includes ion implantation, thin metal plating, etching, and other processes typically used in MEMS fabrication.
- Packaging of MEMS

Training program on  
**MEMS Design using  
IntelliSuite**

**Registration Form**

Name -----

Address -----  
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Phone -----

E-mail -----

Signature-----

Accommodation needed: Yes / No

Demand Draft information:

Date -----

**Eligibility for registration**

BE / B Tech 3<sup>rd</sup> and 4<sup>th</sup> year, M Sc and M  
Tech students

**Duration of the Course**

8<sup>th</sup> and 9<sup>th</sup> September, 2010.

**Resource person**

**Mr. Kunal Trivedi,**  
Big tec solutions pvt limited,  
Bangalore,

Registration Fee: ₹ 500 (DD in favour VIT  
university) + accommodation charges (if  
accommodation needed)

**For Registration please contact:**

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8<sup>th</sup> and 9<sup>th</sup> September, 2010

Organized  
by

**NPMASS sponsored MEMS  
Design Centre  
School of Electronics  
Engineering**

VIT University  
Vellore-632014, Tamil Nadu, India

[www.vit.ac.in](http://www.vit.ac.in)



**A place to learn, a chance to grow**